What is claimed is:

1. A method of forming a metal line in a semiconductor device, comprising the steps of:

forming an interlay insulating film on a semiconductor substrate in which a lower line is formed;

patterning the interlay insulating film to form an aperture unit for forming an upper line connected to the lower line;

cooling the semiconductor substrate in which the aperture unit is formed at a given temperature;

implementing a cleaning process using a hydrogen reduction reaction in order to remove polymer formed on the sidewall of the aperture unit and a metal oxide film formed on the lower line;

implementing an annealing process in-situ within a chamber in which the cleaning process is implemented; and

burying the aperture unit with a conductive material to form an upper line.

2. The method as claimed in claim 1, wherein the aperture unit is a contact hole, a trench, a single damascene pattern, or a dual damascene pattern consisting of a via hole and a trench.

3. The method as claimed in claim 1, wherein, the cleaning process is implemented using H_2 gas and Ar gas or H_2 gas, Ar gas and N_2 gas at

a low temperature of about 25℃～50℃.

4. The method as claimed in claim 1, wherein the cleaning process is implemented by implanting H_2 gas of 2～15sccm and Ar gas of 4～30sccm at a pressure of 1.5～3mT, a source power of 500～750W and a bias power of 0～100W, or implanting H_2 gas of 2～15sccm, N_2 gas of 2～15sccm and Ar gas of 4～30sccm at a pressure of 1.5～3mT, a source power of 500～750W and a bias power of 0～100W.

5. The method as claimed in claim 1, wherein, the annealing process is implemented in two steps, wherein the first step is implemented at a relatively low temperature of blow 100℃～150℃ in order to mitigate stress and detach OH radicals or H_2O residua absorbed on the sidewall of the aperture unit, and the second step is implemented at a relatively high temperature of about 300℃～400℃ in order to accomplish densification of the interlay insulating film and the lower line.

6. The method as claimed in claim 1, wherein the interlay insulating film is an insulating film of SiOC series having a low dielectric constant.

7. The method as claimed in claim 1, wherein the lower line is a copper film.

8. The method as claimed in claim 1, wherein the cooling process is slowly implemented 10～50℃/min.

9. The method as claimed in claim 1, wherein the step of forming the aperture unit comprises:

etching the interlay insulating film to form a via hole;

burying the via hole with an anti-reflective film; and

etching a part of the interlay insulating film to form a trench having an aperture unit wider than the via hole and exposing the lower line through the via hole.

10. The method as claimed in claim 9, wherein the step of forming the trench and the step of implementing the cleaning process are in-situ implemented.

11. The method as claimed in claim 1, wherein the step of forming the upper line comprises:

depositing a barrier film along the step of the semiconductor substrate in which the aperture unit is formed;

depositing a metal seed layer on the barrier film;

forming a metal film on the metal seed layer using an electroplating method, thus burying the aperture unit; and

polishing the metal film to form an upper line.